

We claim:

1. A switching system, comprising:
 - a clock signal having a rising edge and a falling edge;
 - 2^K data inputs and 2^K data select signals;
 - K layers of switches, wherein each j^{th} layer is configured to receive $2^{K-(j-1)}$ data inputs and propagate 2^{K-j} of the $2^{K-(j-1)}$ data inputs, wherein each j^{th} layer is further configured to receive $2^{K-(j-1)}$ data select signals and propagate 2^{K-j} of the $2^{K-(j-1)}$ data select signals, wherein each layer comprises 2^{K-j} switches, wherein each of the 2^{K-j} switches comprises:
 - a logical OR gate configured to receive at least two select signals and generate a data valid signal;
 - a multiplexer (MUX) configured to receive at least two data input signals and one of the at least two select signals, the MUX further configured to generate a data output;
 - a first flip flop configured to receive the data valid signal and release the data valid signal in response to the rising edge of the clock signal; and
 - a second flip flop configured to receive the data output and release the data output in response to the rising edge of the clock signal.

2. A switching system, comprising:

a clock signal having a rising edge and a falling edge;

switches, wherein each switch comprises:

a logical OR gate configured to receive at least two select signals and

generate a data valid signal;

a multiplexer (MUX) configured to receive at least two data input signals

and one of the at least two select signals, the MUX further configured to generate a data output; and

a first flip flop configured to receive the data valid signal and release the data valid signal in response to the rising edge of the clock signal;

a second flip flop configured to receive the data output and release the data output in response to the rising edge of the clock signal;

up to 2^K data inputs and up to 2^K data select signals;

a first layer of switches having 2^{K-1} switches, wherein the first layer is configured to receive the up to 2^K data inputs and propagate 2^{K-1} of the up to 2^K data inputs, wherein the first layer is further configured to receive the up to 2^K data select signals and propagate 2^{K-1} of the up to 2^K data select signals; and

K-1 additional layers of switches, wherein each j^{th} layer of the K-1 additional layers is configured to receive $2^{K-(j-1)}$ data inputs and propagate 2^{K-j} of the $2^{K-(j-1)}$ data inputs, wherein each j^{th} layer is further configured to receive $2^{K-(j-1)}$ data select signals and propagate 2^{K-j} of the $2^{K-(j-1)}$ data select signals, wherein each K-1 additional layer comprises 2^{K-j} switches.

1 3. A switch comprising:
2 a clock having a clock signal;
3 a logical OR gate having two OR inputs and an OR output;
4 a first flip-flop configured to receive the OR output and propagate the OR output in
5 response to the clock signal;
6 a multiplexer (MUX) having a first MUX input, a second MUX input, a MUX
7 output, and a MUX select, wherein the MUX select is one of the two OR inputs; and
8 a second flip-flop configured to receive the MUX output and propagate the MUX
9 output in response to the clock signal.

1 4. A switch comprising:
2 a logical OR gate configured to receive at least two select signals and generate a
3 data valid signal;
4 a multiplexer (MUX) configured to receive at least two data input signals and one
5 of the at least two select signals, the MUX further configured to generate a data output;
6 a first flip flop configured to receive the data valid signal and release the data valid
7 signal in response to a clock signal; and
8 a second flip flop configured to receive the data output and release the data output
9 in response to the clock signal.

1 5. The system of claim 4, wherein the first flip flop is configured to release the
2 data valid signal in response to a rising edge of the clock signal.

1 6. The system of claim 4, wherein the first flip flop is configured to release the
2 data valid signal in response to a falling edge of the clock signal.

1 7. The system of claim 4, wherein the second flip flop is configured to release
2 the data output in response to a rising edge of the clock signal.

1 8. The system of claim 4, wherein the second flip flop is configured to release
2 the data output in response to a falling edge of the clock signal.

1 9. A system, comprising:
2 data select signals;
3 data inputs; and
4 a switching system configured to receive the data select signals and the data inputs,
5 the switching system further configured to produce a data valid signal in response to the
6 received data select signals, the switching system further configured to generate a data
7 output from the data inputs in response to the data select signals.

1 10. The system of claim 9, wherein the switching system comprises a plurality
2 of switches.

1 11. The system of claim 10, wherein each of the plurality of switches
2 comprises:

3 a logical OR gate configured to receive at least two select signals and generate a
4 data valid signal;

5 a multiplexer (MUX) configured to receive at least two data input signals and one
6 of the at least two select signals, the MUX further configured to generate a data output;

7 a first flip flop configured to receive the data valid signal and release the data valid
8 signal in response to a clock signal; and

9 a second flip flop configured to receive the data output and release the data output
10 in response to the clock signal.

1 12. The system of claim 11, wherein the first flip flop is configured to release
2 the data valid signal in response to a rising edge of the clock signal.

1 13. The system of claim 11, wherein the first flip flop is configured to release
2 the data valid signal in response to a falling edge of the clock signal.

1 14. The system of claim 11, wherein the second flip flop is configured to
2 release the data output in response to a rising edge of the clock signal.

1 15. The system of claim 11, wherein the second flip flop is configured to
2 release the data output in response to a falling edge of the clock signal.

- 1 16. A switching method comprising the steps of:
- 2 (a) receiving a number of data inputs and a number of data select signals,
- 3 wherein the number of data inputs and the number of data select signals is the same;
- 4 (b) choosing at least half of the received data inputs and at least half of the
- 5 received data select signals, wherein the chosen number of data inputs and the chosen
- 6 number of data select signals is the same, wherein the at least half of the received data
- 7 inputs and at least half of the received data select signals is a power of 2;
- 8 (c) outputting the chosen data inputs and the chosen data select signals;
- 9 (d) sequentially repeating steps (a) through (c) until only one data input and
- 10 only one data select signal is outputted.

- 1 17. A method comprising the steps of:
- 2 (a) receiving a number of data inputs;
- 3 (b) choosing at least half of the received data inputs; and
- 4 (c) outputting the chosen data inputs.

- 1 18. The method of claim 17, wherein the step of choosing at least half of the
- 2 received data inputs comprises the step of selecting a number of received data inputs such
- 3 that the selected number of received data inputs is a power of 2.

- 1 19. The method of claim 17, further comprising the step of repeating steps (a)
- 2 through (c) until only one data input is outputted.

- 1 20. The method of claim 17, further comprising the steps of:
- 2 (d) receiving a number of data select signals;
- 3 (e) choosing at least half of the received data select signals; and
- 4 (f) outputting the chosen data select signals.

- 1 21. The method of claim 20, wherein the step of choosing at least half of the
- 2 received data select signals comprises the step of selecting a number of received data
- 3 selects signals such that the selected number of received data select signals is a power of 2.

- 1 22. The method of claim 20, further comprising the step of repeating steps (d)
- 2 through (f) until only one data select signal is outputted.

- 1 23. The method of claim 20, wherein step (d) and step (f) are responsive to a
- 2 clock signal having a rising edge and a falling edge.

- 1 24. The method of claim 23, wherein step (d) and step (f) are further responsive
- 2 to the rising edge of the clock signal.

- 1 25. The method of claim 23, wherein step (d) and step (f) are further responsive
- 2 to the falling edge of the clock signal.

1 26. A switching system comprising:
2 means for receiving a number of data inputs and a number of data select signals,
3 wherein the number of data inputs and the number of data select signals is the same;
4 means for choosing at least half of the received data inputs and at least half of the
5 received data select signals, wherein the chosen number of data inputs and the chosen
6 number of data select signals is the same, wherein the at least half of the received data
7 inputs and at least half of the received data select signals is a power of 2; and
8 means for outputting the chosen data inputs and the chosen data select signals;

1 27. A switch comprising:
2 means for receiving a number of data inputs;
3 means for choosing at least half of the received data inputs; and
4 means for outputting the chosen data inputs.

1 28. The switch of claim 27, wherein the means for choosing at least half of the
2 received data inputs comprises means for selecting a number of received data inputs such
3 that the selected number of received data inputs is a power of 2.

1 29. The switch of claim 27, further comprising:
2 means for receiving a number of data select signals;
3 means for choosing at least half of the received data select signals; and
4 means for outputting the chosen data select signals.

1 30. The switch of claim 29, wherein the means for choosing at least half of the
2 received data select signals comprises means for selecting a number of received data
3 selects signals such that the selected number of received data select signals is a power of 2.

1 31. A switch comprising:
2 means for receiving at least two select signals;
3 means for generate a data valid signal from the at least two select signals;
4 means for receiving at least two data input signals and one of the at least two select
5 signals;
6 means for generating a data output from the at least two data input signals in
7 response to the one of the at least two select signals;
8 means for receiving the data valid signal;
9 means for releasing the data valid signal in response to a clock signal;
10 means for receiving the data output; and
11 means for releasing the data output in response to the clock signal.

- 1 32. A system, comprising:
- 2 data select signals;
- 3 data inputs; and
- 4 means for receiving the data select signals and the data inputs;
- 5 means for producing a data valid signal in response to the received data select
- 6 signals; and
- 7 means for generating a data output from the data inputs in response to the data
- 8 select signals.